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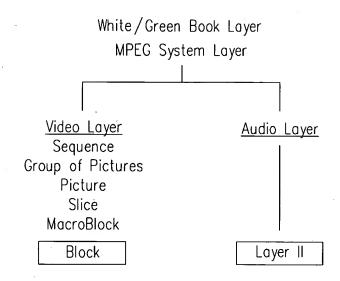


FIG. 1

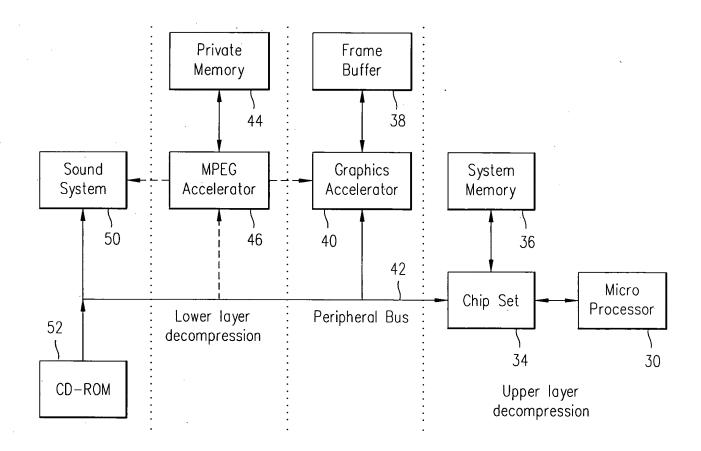


FIG. 2

2/11

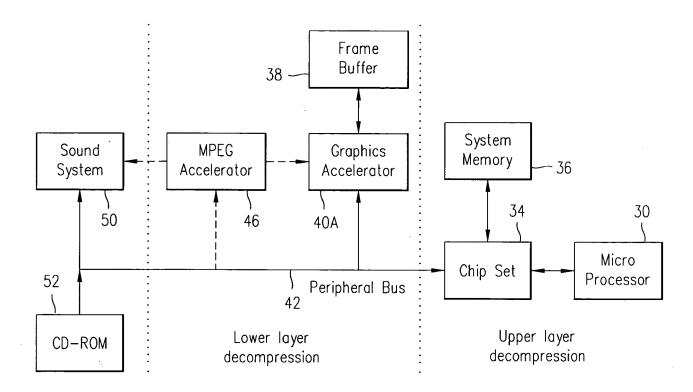


FIG. 3

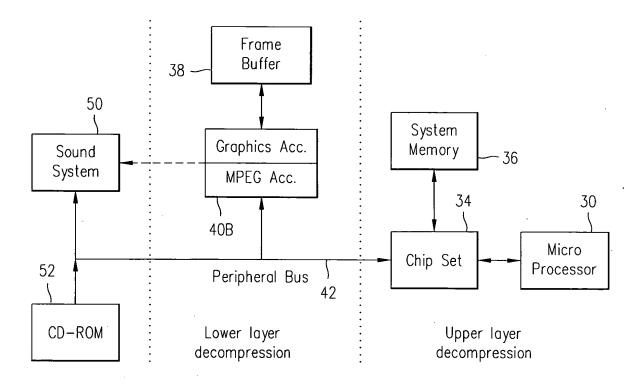
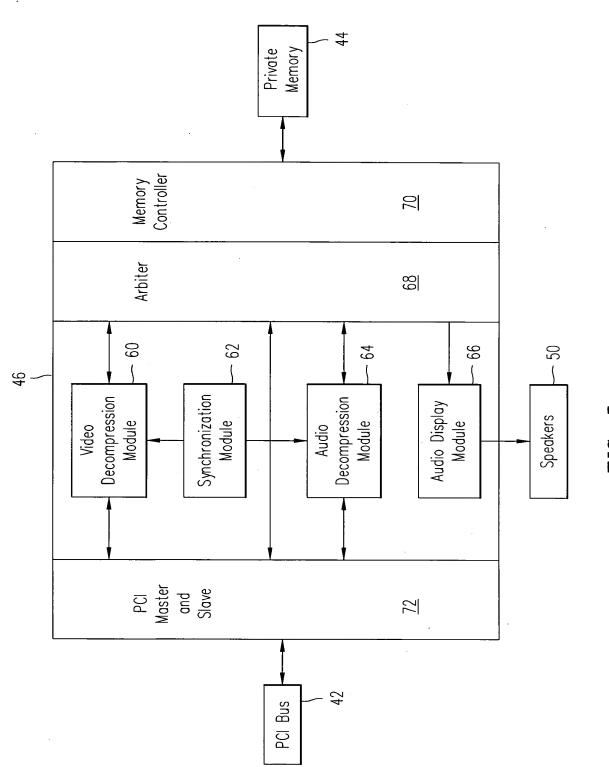


FIG. 4





F.IG. 5

4/11

	art Sto ime Fra					art ame
Display			display IO frame	display B1 frame	display B2 frame	display P3 frame
VDE	decode IO frame	decode P3 frame	decode B1 frame	decode B2 frame	decode P6 frame	decode B4 frame
Host (Software) Driver	P3 Program	B1 Program	B2 Program	P6 Program	B4 Program	B5 Program

FIG. 6

						tart ame
Display			display IO frame	no display B1 frame	display B2 frame	display P3 frome
VDE	decode IO frame	decode P3 frame	decode B1 frame	decode B2 frame	decode P6 frame	decode B4 frame
Host (Software) Driver	P3 Program	B1 Program	abandon B1 frame B2 Program	P6 Program	B4 Program	

FIG. 7

5/11

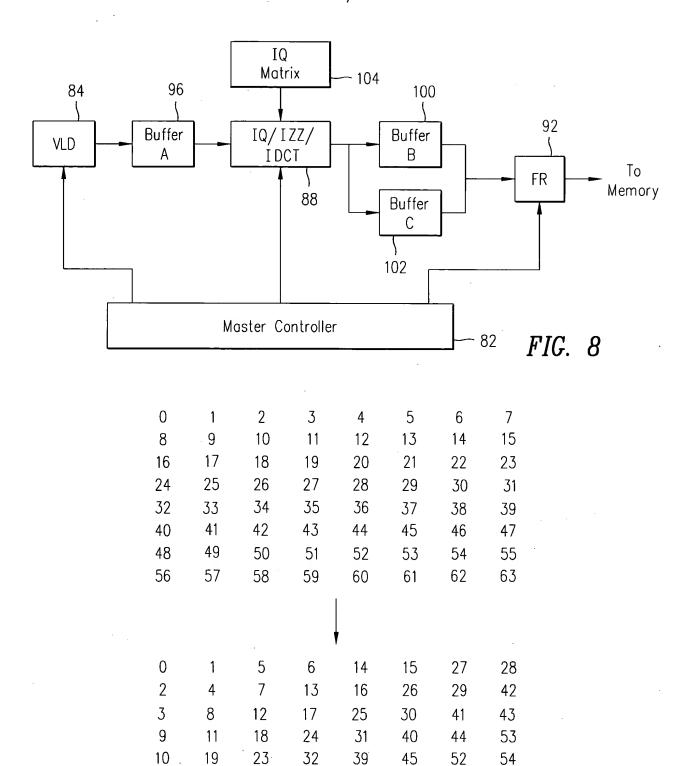
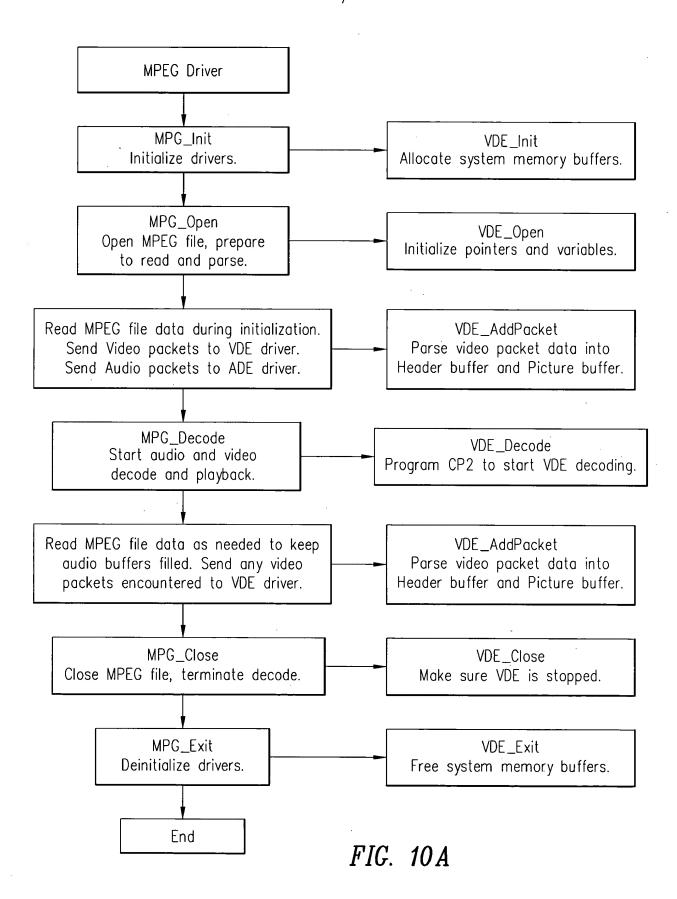


FIG. 9

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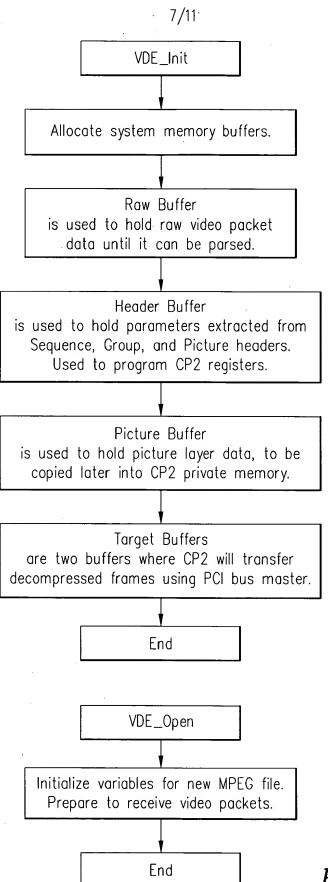
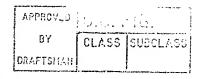


FIG. 10B



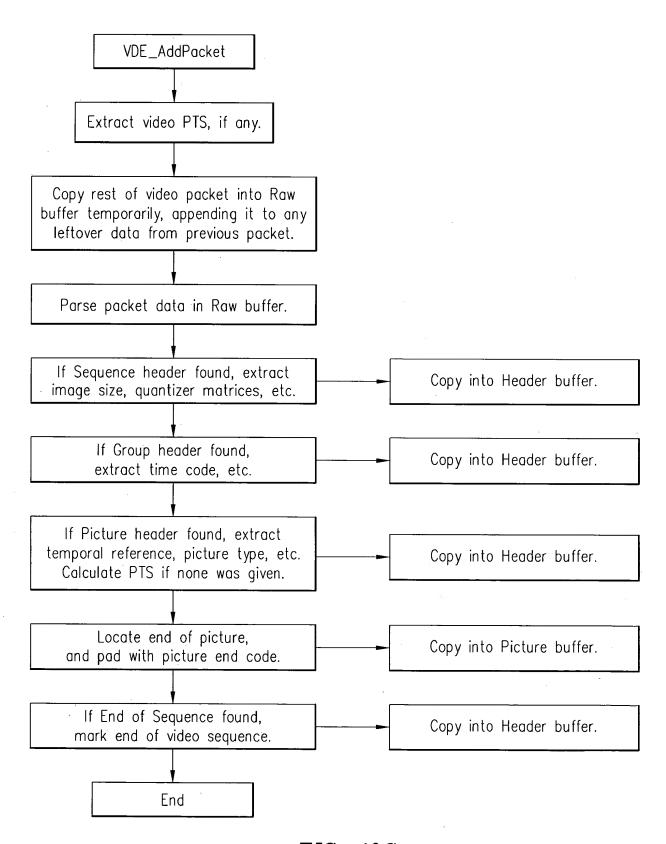


FIG. 10C

· 9/11

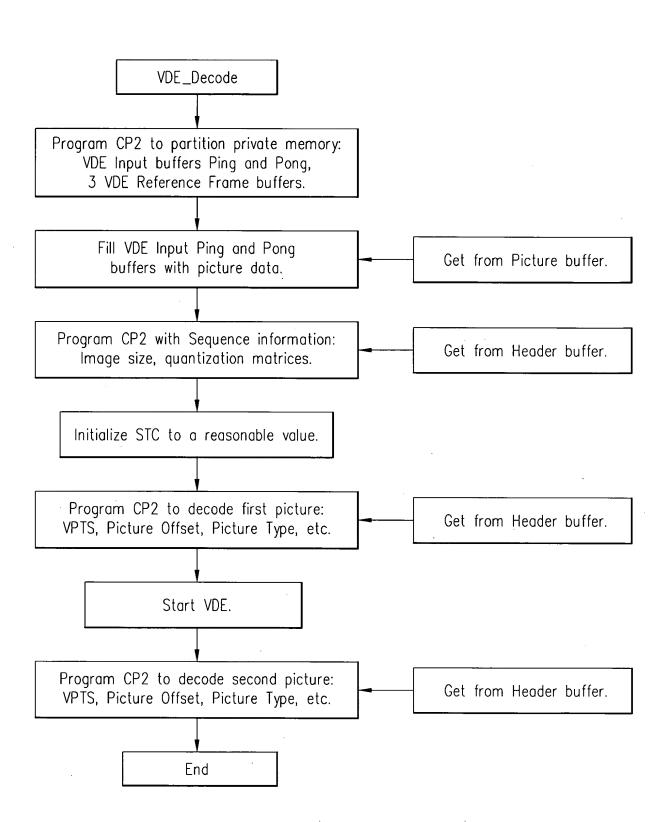


FIG. 10D

APPROVED | U.G. FIG.

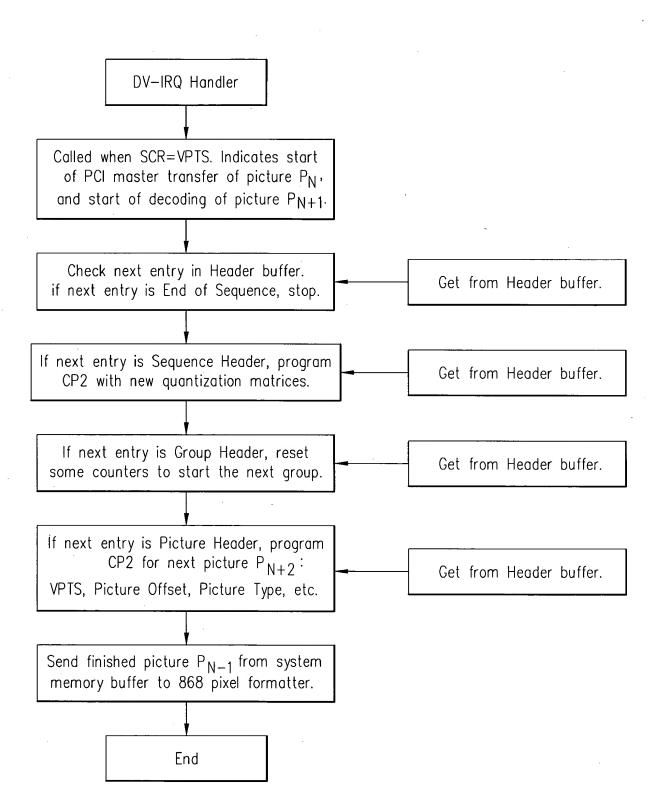


FIG. 10E

APPROVED U.G. FIG.

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